TWO-BIT SPLIT-GATE NON-VOLATILE MEMORY TRANSISTOR

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ABSTRACT OF THE DISCLOSURE

A 2-bit non-volatile memory (NVM) transistor having a pair of isolated floating gate electrodes is provided. One of the floating gate electrodes is located over a first source/drain region, and a first adjacent end of a channel region. The other floating gate electrode is located over a second source/drain region and a second adjacent end of the channel region. A control gate extends over both floating gate electrodes and a centrally located portion of the channel region. The floating gate electrodes are independently programmed and independently read, thereby enabling the NVM transistor to effectively store 2-bits of data.